AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. (Original) A method comprising:

determining an offset between a first clock signal and a second clock signal, the first clock signal having a first frequency related to a reference clock and the second clock signal having a second frequency different from the first frequency and related to the reference clock;

determining an effective phase shift between the first clock signal and the second clock signal, the effective phase shift representing a smallest interval between a reference edge of the first clock signal and an immediately adjacent reference edge of the second clock signal; and

determining an edge difference based on the effective phase shift.

2. (Original) The method of claim 1 further including adjusting an interval between a reference edge of a first test clock signal and a reference edge of a second test clock signal to simulate worst case slack.

3. (Original) The method of claim 2 wherein the worst case slack is worst case setup slack.

4. (Original) The method of claim 2 wherein the worst case slack is worst case hold slack.

5. (Original) The method of claim 1 wherein determining an edge difference for worst case slack includes setting the edge difference equal to the effective phase shift.

6. (Original) The method of claim 5 wherein setting the edge difference equal to the effective phase shift is performed if the effective phase shift is non-zero.

7. (Original) The method of claim 1 wherein determining an effective phase shift includes determining a greatest common divisor of the first clock signal and the second clock signal.

8. (Original) The method of claim 7 wherein determining an effective phase shift includes setting the effective phase shift equal to *MOD(Offset, GCD(Mx, Mr))*.

9. (Original) The method of claim 1 wherein determining an offset includes determining a non-negative offset.

10. (***Canceled***)

11. (***Currently Amended***) ~~The technique of claim 10~~ A technique for use in static timing analysis of a circuit employing a transmit clock and a receive clock having different frequencies related to a frequency of a common reference clock, the technique to account for a phase difference between the transmit clock and the receive clock, the technique comprising:

determining an offset between the transmit clock and the receive clock;

determining an effective phase shift between the transmit clock and the receive clock, the effective phase shift representing a smallest interval between a reference point on the transmit clock and an immediately adjacent corresponding reference point on the receive clock, and

setting an edge difference equal to the effective phase shift.

12. (Original) The technique of claim 11 wherein the edge difference is set equal to the effective phase shift if the effective phase shift is non-zero.

13. (Original) The technique of claim 11 further comprising adjusting an interval between a reference point on a test transmit clock and a reference point on a test receive clock to simulate the worst case slack.

14. (Original) The technique of claim 13 wherein the worst case slack is worst case setup slack.

15. (Original) The technique of claim 13 wherein the worst case slack is worst case hold slack.

16. (Original) The technique of claim 11 wherein determining an effective phase shift includes setting the effective phase shift equal to *MOD(Offset, GCD(Mx, Mr))*.

17. (Original) A technique for use in static timing analysis of a circuit employing a transmit clock and a receive clock having different frequencies related to a frequency of a common reference clock, the technique to determine a test edge difference corresponding to worst case slack without enumerating triggering events of the transmit clock and the receive clock.

18. (Original) The technique of claim 17 wherein determining a worst case slack includes:

determining an offset between the transmit clock and the receive clock;

determining an effective phase shift between the transmit clock and the receive clock, the effective phase shift representing a smallest interval between a reference point on the transmit clock and an immediately adjacent corresponding reference point on the receive clock; and

setting the test edge difference equal to the effective phase shift.

19. (***Currently Amended***) The technique of claim ~~18wherein~~ 18 wherein the edge difference is set equal to the effective phase shift if the effective phase shift is non-zero.

20. (Original) The technique of claim 18 further comprising adjusting an interval between a reference point on a test transmit clock and a reference point on a test receive clock to simulate the worst case slack.

21. (Original) The technique of claim 20 wherein the worst case slack is worst case setup slack.

22. (Original) The technique of claim 20 wherein the worst case slack is worst case hold slack.

23. (Original) The technique of claim 18 wherein determining a test edge difference includes determining a greatest common divisor of the transmit clock and the receive clock.

24. (Original) The technique of claim 23 wherein determining an effective phase shift includes setting the effective phase shift equal to *MOD(Offset, GCD(Mx, Mr))*.

25. (***Currently Amended***) A computer readable medium tangibly encoding a program of instructions, said program of instructions comprising:

at least one executable instruction to determine an offset between a first clock signal and a second clock signal, the first clock signal having a first frequency related to a reference clock and the second clock signal having a second frequency different from the first frequency and related to the reference clock;

at least one executable instruction to determine an effective phase shift between the first clock signal and the second clock signal, the effective phase shift representing a smallest interval between a reference edge of the first clock signal and an immediately adjacent reference edge of the second clock signal; and

at least one executable instruction to determine an edge difference based on the effective phase shift.

26. (Original) The computer readable medium of claim 25 further including at least one executable instruction to adjust an interval between a reference edge of a first test clock signal and a reference edge of a second test clock signal to simulate worst case slack.

27. (Original) The computer readable medium of claim 26 wherein the worst case slack is worst case setup slack.

28. (Original) The computer readable medium of claim 26 wherein the worst case slack is worst case hold slack.

29. (Original) The computer readable medium of claim 25 wherein the at least one executable instruction to determine a worst case slack includes at least one executable instruction to set the edge difference equal to the effective phase shift.

30. (Original) The computer readable medium of claim 25 wherein the at least one executable instruction to determine a worst case slack includes at least one executable instruction to set the edge difference equal to the effective phase shift if the effective phase shift is non-zero.

31. (Original) The computer readable medium of claim 25 wherein the at least one executable instruction to determine an effective phase shift includes the at least one executable instruction to determine a greatest common divisor of the first clock signal and the second clock signal.

32. (Original) The computer readable medium of claim 31 wherein the at least one executable instruction to determine an effective phase shift includes the at least one executable instruction to set the effective phase shift equal to *MOD(Offset, GCD(Mx, Mr))*.

33. (Original) A method of making a computer readable medium product that encodes an integrated circuit design, the method comprising:

determining an offset between a first clock signal and a second clock signal, the first clock signal having a first frequency related to a reference clock and the second clock signal having a second frequency different from the first frequency and related to the reference clock;

determining an effective phase shift between the first clock signal and the second clock signal, the effective phase shift representing the smallest interval between a reference edge of the first clock signal and an adjacent reference edge of the second clock signal;

determining an edge difference based on the effective phase shift;

generating a circuit design using the worst case slack; and

encoding the circuit design onto the computer readable medium product.

34. (Original) The method of claim 33 further including adjusting an interval between a reference edge of a first test clock signal and a reference edge of a second test clock signal to simulate worst case slack.

35. (Original) The method of claim 33 wherein determining an effective phase shift includes determining a greatest common divisor of the first clock signal and the second clock signal.

36. (Original) The method of claim 35 wherein determining an effective phase shift includes setting the effective phase shift equal to *MOD(Offset, GCD(Mx, Mr))*.

37. (Original) A system comprising:

means for determining an offset between a first clock signal and a second clock signal, the first clock signal having a first frequency related to a reference clock and the second clock signal having a second frequency different from the first frequency and related to the reference clock;

means for determining an effective phase shift between the first clock signal and the second clock signal, the effective phase shift representing a smallest interval between a reference edge of the first clock signal and an adjacent reference edge of the second clock signal; and

means for determining an edge difference based on the effective phase shift.

38. (Original) The system of claim 37 further including means for adjusting an interval between a reference edge of a first test clock signal and a reference edge of a second test clock signal to simulate worst case slack.

39. (Original) The system of claim 38 wherein the worst case slack is worst case setup slack.

40. (Original) The system of claim 38 wherein the worst case slack is worst case hold slack.

41. (Original) The system of claim 37 wherein the edge difference determination means includes means for setting the edge difference equal to the effective phase shift.

42. (Original) The system of claim 41 wherein the means for setting the edge difference sets the edge difference equal to the effective phase shift if the effective phase shift is non-zero.

43. (Original) The system of claim 37 wherein the effective phase shift means includes means for determining a greatest common divisor of the first clock signal and the second clock signal.

44. (Original) The system of claim 43wherein the effective phase shift means includes means for setting the effective phase shift equal to *MOD(Offset, GCD(Mx, Mr))*.

45. (Original) The system of claim 37 wherein the offset means includes means for determining a non-negative offset.